Amendments to the Specification:

Please replace paragraph [0037] with the following amended paragraph:

[0037] As shown in [[Fig.]] Fig. 10, [[Fig.]] Fig. 10 is a cross-sectional diagram of a (+/-) HVMOS device 402 and a Submicron MOS device 404 formed on a silicon substrate 400 according to the present invention method . The only difference between Fig.10 and Fig.3 is that one step to form a deep well region of a the Submicrom MOS device 404 having an opposite conductivity conductive type with a conductivity type to the silicon substrate 400 is performed. First, the N-type deep well region 478 of an HVMOS device 302 comprising a well region 306 of a first conductivity type and athe Submicron MOS device 404 is comprising formed, and then a P-type well region 406 of the HVMOS device 402 are all is formed on the P-type silicon substrate 400. 300 The deep well region 478 having the opposite a conductive type to the silicon substrate 400 in order to prevents a back bias effect between anthe HVMOS device 402 and athe Submicron MOS device 404. After that, a plurality of shallow trenches 412,414,416,418,434,436 are formed and all the subsequent steps are the same as those previously described in Fig.4 to Fig.9.